# Structural and electrical investigations of graphene / 3C-SiC heterostructures elaborated by CVD on (111) and (100) silicon substrates

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The past decade has seen the emergence of graphene as a promising material for developing high frequency electronic applications. But before the future graphene based devices can compete with the current Si technology major challenges must be overcome. Among them, the formation of nanoscale graphene domains, suitable for the realisation of ambipolar devices, puts light on the importance both of the elaboration method and the substrate on which graphene is obtained. If bulk hexagonal Silicon Carbide ($\alpha$-SiC) substrates have demonstrated a high efficiency for obtaining tuneable graphene structures [1], their relatively high cost with respect to Silicon as well as their limited diameter size constitute major issues regarding a widespread dissemination of a graphene based technology. In this perspective, cubic-SiC ($\beta$-SiC or 3C-SiC) epilayers grown on silicon recently gained interest since the ability to produce graphene films on such templates has been demonstrated under ultra high vacuum environment [2-4].

In this way, this work aims to discuss the structural and electrical properties of graphene films elaborated on 3C-SiC/Si templates. Contrary to the previous cited works [2-4], graphene films under consideration in this contribution have been elaborated under Chemical Vapour Deposition (CVD) environment, using a derived approach from that we recently proposed to perform direct epitaxy of graphene on 6H-SiC [7]. It has been demonstrated that such a CVD environment is more efficient to produce high quality graphene but, to date, only using bulk h-SiC substrates [5-6].

For this work, 3C-SiC epilayers were previously grown on 2inches silicon substrates oriented along (111) and (100) crystalline directions. Deposition was done in a resistively heated hot wall Chemical Vapour Deposition chamber with classical two steps deposition process (carbonization / growth) using silane and propane as precursors diluted in hydrogen. After deposition, epilayers are released to air for characterization and, for some cases, polishing before graphitization process. This last is done in the same reactor used for 3C-SiC elaboration. The 3C-SiC epilayers are annealed at 1300°C under a mixture of argon and propane during 30-60min at a pressure ranging from 6 to 600mbar. After thermal annealing, structural properties of the graphene/graphite surface phase were investigated by means of Low Energy Electron Diffraction (LEED), Atomic Force Microscopy (AFM), X ray Photoemission Spectroscopy (XPS) and Raman Spectroscopy. Basic electrical properties of the surface after thermal treatment have been measured in a second time by using the circular-Transfer Length Method (c-TLM). For that purpose, Ti/Au (30/200nm) films have been deposited in an e-beam evaporator using standard lithography and lift off process to reveal c-TLM patterns. In order to benchmark the graphitization mechanism, the same graphitization processes have been applied to Si terminated 6H-SiC substrates.

In a first time, we briefly introduce the structural properties of the 3C-SiC/Si templates used for the study. So we discuss in details the formation of the surface graphitic phase, for both (100) and (111) crystalline orientations. That is attested by XPS and Raman where typical spectral features attributed to sp2 carbon linked network are observed after graphitization process. The intrinsic differences of the graphitization process applied to the two differently oriented 3C-SiC/Si templates are presented. Basing on XPS and Raman data, it is demonstrated that a more ordered graphitization mechanism, leading to

the formation of graphene films similarly to the Si terminated face of 6H-SiC substrates, is obtained on (111) faces. In case of (100) faces, the graphitic phase which is formed subsequently to graphitization process is more rapidly achieved than on (111) faces but is accompanied by a lower degree of organization (see Fig. 1). It is also shown that a good homogeneity of the graphene formation on the whole 2inches template is achieved. The case of polished 3C-SiC(111) epilayers is also discussed. Finally we present the electrical characterizations performed on both orientations. The influence of the 3C-SiC underlying film on the electrical properties obtained (specific contact resistance and sheet resistance, $\rho_c$ and $R_{sh}$) is discussed and compared to that obtained with graphene on 6H-SiC substrates (see Fig. 2).

In summary, our contribution demonstrates the elaboration of graphene films on 2inches 3C-SiC/Si templates using a CVD approach. We show that structural differences exist between both crystalline orientations and are investigated. We also present some basic electrical measurements which reveal the ohmic character of the contact on graphitic phase / 3C-SiC and indication of a better conductivity of graphitic phase obtained on 3C-SiC(100) films despite a lower surface crystalline arrangement. This contribution allows to substantiate a low cost approach of graphene formation which could be suitable for integrating graphene within Si technology.

## References


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## Figures

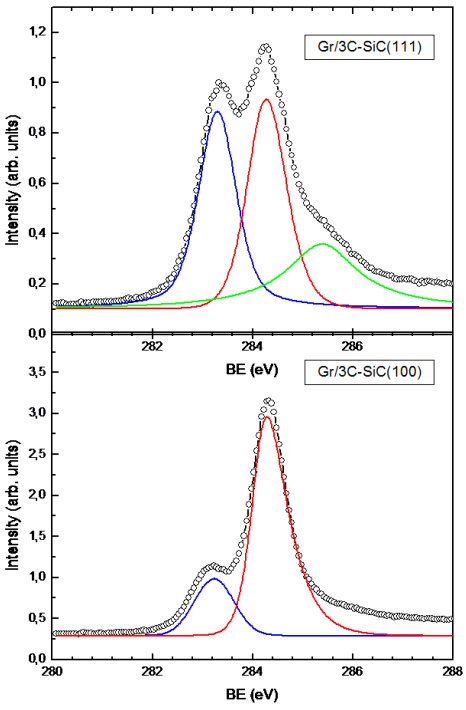


Fig 1 : XPS analysis of the CVD graphitization mechanism on 3C-SiC(111) and 3C-SiC(100) templates, under the same experimental conditions.

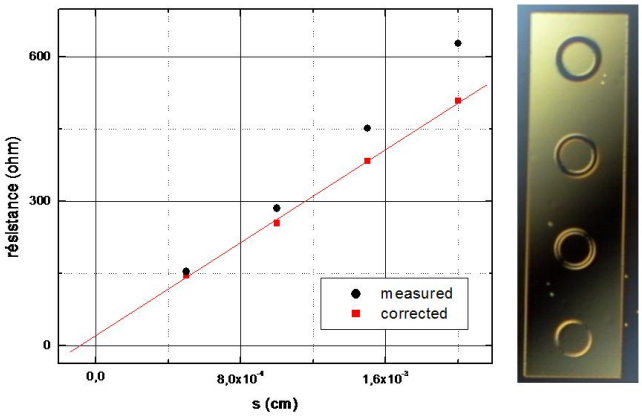


Fig 2: Determination of $\rho_c$ and $R_{sh}$ by c-TLM method. Left: experimental measures; right, c-TLM patterns